

IN THE CLAIMS:

Please cancel claims 22, 25, 29, 32, 23, 26, 30, 33 - 35, and 39 - 41. For convenience all claims are presented.

- 1 21. An inspection system comprising:
 - 2 an inspection apparatus for detecting positions and sizes of particles or
 - 3 pattern defects on an object to be inspected;
 - 4 an image taking apparatus for taking images of said particles or said
 - 5 pattern defects as detected by said inspection apparatus; and
 - 6 an analysis unit operatively coupled to said inspection apparatus and said
 - 7 image taking apparatus, said analysis unit including:
 - 8 a storage device for storing therein inspection data produced by
 - 9 said inspection apparatus and position information of regions of a circuit pattern to be
 - 10 formed on said object;
 - 11 a calculation device for identifying particles and pattern defects
 - 12 that are correspondingly positioned in said regions, and calculating failure probabilities
 - 13 for said particles and said pattern defects positioned in said regions based on their sizes;
 - 14 and
 - 15 a selection device for selecting particles or pattern defects whose
 - 16 calculated failure probabilities are greater than or equal to a predetermined threshold.

22 - 23. These claims have been canceled in response to a restriction.

- 1 24. The inspection system according to claim 21, wherein said regions
- 2 are circuit blocks as formed within an LSI chip.

25 - 26. These claims have been canceled in response to a restriction.

- 1 27. The inspection system according to claim 21, further comprising a
- 2 simulation device for generating virtual defects at random positions with respect to circuit
- 3 graphics obtainable from mask layout data forming said circuit pattern, and computing

4 said failure probabilities from connection relationships of said circuit graphics and said
5 defects.

1 28. The inspection system according to claim 21, wherein said position
2 information of said regions is generated from mask layout data forming an LSI chip.

29 - 30. These claims have been canceled in response to a restriction.

1 31. The inspection system according to claim 24, wherein said position
2 information of said circuit blocks is generated from mask layout data forming an LSI
3 chip.

32 - 35. These claims have been canceled in response to a restriction.

1 36. A method for manufacturing semiconductor devices comprising
2 the steps of:

3 a fabrication step for forming circuit patterns on or over a wafer, said
4 circuit patterns constituting a plurality of semiconductor chips;

5 an inspection step for detecting positions and sizes of particles or pattern
6 defects of said wafer;

7 identifying positions and sizes of those of said particles or said pattern
8 defects located in a region of said circuit patterns that constitute one of said
9 semiconductor chips;

10 a calculation step for calculating failure probabilities based on sizes of
11 said pattern defects in said region;

12 an extraction step for extracting positions of said particles or said pattern
13 defects with calculated failure probabilities greater than or equal to a predefined
14 threshold; and

15 producing images of said particles or said pattern defects extracted at said
16 extraction step.

1 37. A method for manufacturing semiconductor devices according to
2 claim 36, wherein said regions are circuit blocks within an LSI chip.

1 38. A method for manufacturing semiconductor devices according to
2 claim 37, wherein said LSI chip is a system LSI and said circuit blocks include memory
3 portions and logic portions.

39 - 41. These claims have been canceled in response to a restriction.